In the Claims.

1. (Amended) A semiconductor apparatus, comprising:

a plurality of device elements formed on a surface of a semiconductor substrate, each device element having a diffusion region; and

a multi-layer wiring configuration electrically connecting at least two of the diffusion regions, the multi-layer wiring configuration containing a plurality of wiring layers, a first one of the plurality of wiring layers being divided into a first wiring region for providing wiring in a first direction and a second wiring region for providing wiring in a second direction.

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3. (Amended) The semiconductor apparatus according to claim 2, wherein:

predetermined wiring in the first one of the plurality of wiring layers is electrically connected to and disposed in parallel with wiring in a second one of the plurality of wiring layers; and

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the second one of the plurality of wiring layers has a higher sheet resistance than the first one of the plurality of wiring layers.

4. (Amended) The semiconductor apparatus according to claim 2, wherein the first one of the plurality of wiring layers includes:

a first wiring trace in the second wiring region disposed in the second direction;

a second wiring trace in the second wiring region disposed in the second direction and separated from the first wiring trace in the first direction; and

a third wiring trace in the first wiring region disposed in the first direction and electrically connecting the first wiring trace and the second wiring trace.

5. (Amended) The semiconductor apparatus according to claim 2, further including:

the multi-layer wiring configuration includes a second one of the plurality of wiring layers;

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a memory array having bit lines formed with bit line wiring layers of the same material as the second one of the plurality of wiring layers; and

the second one of the plurality of wiring layers has a higher sheet resistance than the first one of the plurality of wiring layers.

7. (Amended) A semiconductor apparatus, comprising:

a plurality of functional circuit blocks, each functional circuit block including a plurality of device elements, a first wiring region and a second wiring region; and

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a multi-layer wiring configuration containing a plurality of wiring layers for electrically connecting predetermined ones of the device elements, the multi-layer wiring configuration including a first one of the plurality of wiring layers disposed in the first wiring region providing first wiring in a first direction and the first one of the plurality of wiring layers disposed in the second wiring region providing second wiring in a second direction.

9. (Amended) The semiconductor apparatus according to claim 8, comprising:

a predetermined first portion of the first one of the plurality of wiring layers is electrically connected to and disposed in parallel with wiring in a second one of the plurality of wiring layers of the plurality of wiring layers; and

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the second one of the plurality of wiring layers has a higher sheet resistance than the first one of the plurality of wiring layers.

10. (Amended) The semiconductor apparatus according to claim 9, wherein the second one of the plurality of wiring layers has a higher melting point than the first one of the plurality of wiring layers.

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12. (Amended) The semiconductor apparatus of claim 8, further including:

the multi-layer wiring configuration includes a second one of the plurality of wiring layers;

a memory array having bit lines formed with bit line wiring layers of the same material as the second one of the plurality of wiring layers; and

the second one of the plurality of wiring layers has a higher sheet resistance than the first one of the plurality of wiring layers.

13. (Amended) The semiconductor apparatus of claim 8, wherein the device elements are insulated gate field effect transistors (IGFETs), each IGFET having a source/drain diffusion region and the multi-layer wiring structure electrically connects a source/drain region of at least two IGFETs within a functional circuit block by using the first one of the plurality of wiring layers in the first wiring region and the second wiring region.